THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 27

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WOODROW L. MEEKER

Appeal No. 1997-2059
Application 08/112,540[1]

Heard: October 06, 1999

Before HAIRSTON, HECKER and GROSS, Administrative Patent Judges.

HECKER, Administrative Patent Judge.

DECISION ON APPEAL

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[1] Application for patent filed August 27, 1993.

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This is a decision on appeal from the final rejection of claims 1 through 33. Claims 11, 13, 22 and 30 have been canceled by an amendment after final rejection, paper no. 11. Claims 1, 2, 12, 18, 23, 26 and 31 were subsequently indicated as allowable in the Examiner's answer at page 4.

The invention relates to parallel processor integrated circuit component, and more particularly to a Single Instruction Multiple Data (SIMD) array processing unit. An array of processing cells performs logical or arithmetic operations on its own data at the same time that all other cells are processing their own data. At every instant the same instruction is supplied to each of the cells so that the logical or arithmetic operation being performed at any instant in time is identical for all cells in the array. Although SIMD arrays may be based upon the same generic concepts, design details can have a great impact on processing cost and circuit performance. Appellant's invention optimizes the arrangement of the Arithmetic Logic Unit (ALU), Random Access Memory (RAM), global signal generator, identity of equality of multibit operands, and cell bypass.

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

Representative independent claim 6 is reproduced as follows:

6. A parallel processor comprising:
control input means for receiving control signals; and

a plurality of identical processing cells, each of the processing cells being connected to at least one neighboring cell and to the control input means for processing data in accordance with the control signals;

wherein each of the processing cells comprises:

an arithmetic logic unit (ALU) having an output representing a carry bit from an arithmetic operation; and

addressable memory means coupled to receive and store the carry bit from the ALU output in response to a control signal received by the control input means,

wherein:

the addressable memory means comprises a plurality of storage locations and an address port for receiving an address signal, the address signal selecting one of the storage locations for use in a write or read operation of the addressable memory means; and

the carry bit from the ALU output is routed to the addressable memory means without passing through any intervening clockable storage means.

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

The Examiner relies on the following references:

Batcher	4,314,349	Feb. 2, 1982
Morton	4,546,428	Oct. 8, 1985
Holsztynski	4,739,474	Apr. 19, 1988
Guttag et al. (Guttag)	4,752,893	Jun. 21, 1988
Holsztynski et al.(Holsztynski)	5,421,019	May 30, 1995 (filed Sep. 23, 1992)

Claims 3, 7 through 10, 19, 21, 27 and 29 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Holsztynski et al. which incorporates by reference Holsztynski. Claims 4 through 6, 20 and 28 stand rejected under 35 U.S.C.

§ 103 as being unpatentable over Holsztynski et al. (which incorporates Holsztynski) in view of Morton. Claims 16, 17, 25 and 33 stand rejected under 35 U.S.C. § 103 as being unpatentable over Batcher. Claims 14, 15, 24 and 32 stand rejected under 35 U.S.C. § 103 as being unpatentable over Batcher in view of Guttag.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the brief, reply brief and answer for the respective details thereof.

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

OPINION

After a careful review of the evidence before us, we will not sustain the rejection of claims 3, 7 through 10, 19, 21, 27 and 29 under 35 U.S.C. § 102(e), nor will we sustain the rejection of claims 4, 5, 6, 14 through 17, 20, 24, 25, 28, 32 and 33 under 35 U.S.C. § 103.

Although the Examiner has cited prior art teachings of the basic concepts claimed by Appellant, the Examiner not shown the particular implementation claimed.

35 U.S.C. § 102(e) Rejection

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. See In re King, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). "Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984),

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

cert. dismissed, 468 U.S. 1228 (1984), citing Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 772, 218 USPQ 781, 789 (Fed. Cir. 1983). With regard to the rejection of independent claim 3, Appellant argues:

> Neither of the Holsztynski '019 and '474 patents can be relied upon as an anticipating reference under section 102 because neither discloses an ALU that produces a single signal that is capable of alternatively supplying a CARRY or a BORROW signal **in dependence on the value of a control signal**. (Emphasis added.) (Brief-page 23.)

The Examiner's response on page 10 of the Answer disputes the label ALU in claim 3, "implying NOT an Arithmetic Logic Unit but an arithmetic unit such as an adder." However, this does not address the limitation of "the output [of the ALU] selectively representing either a carry or a borrow result...**in response to a first control signal received by the control means**." (emphasis added) as recited in claim 3. Nowhere does the Examiner address this limitation. Thus, although Holsztynski et al. does show ALU 110 in Figure 4(a), it does not show the implementation claimed by Appellant and depicted as ALU 444 in Figure 4, with the carry/borrow select signal CW(21). For this reason, we will not sustain the 35 U.S.C. § 102(e) rejection of

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

claim 3, and likewise claims 19 and 27 which depend therefrom and incorporate the same unmet limitation.

With regard to independent claim 7, Appellant argues:

> Nowhere, however, does Holsztynski '019 describe routing the global GLOR signal back into the cell through global signal input means exclusively for receiving the global signal from the global signal generating means, as recited in the claim. This may readily be seen by examining Holsztynski '019's FIGS. 4(a) & 4(b): The GLOBAL signal is shown as an output signal from the cell in FIG. 4(b), but nowhere is a processing cell input means shown for receiving this signal. The Holsztynski patents also fail to disclose any memory means for storing a global signal from global signal input means. (Brief-page 25.)

The Examiner responds:

> Holsztynski ('019) discloses global signal (GLOR) generation circuitry shown in Figure 4b (element 150) and described in Col. 5, line 61 et seq. (Answer-page 10.)

Again, as with claim 3 supra, the Examiner presents art with the basic concept, but not Appellant's claimed implementation. Claim 7 recites "global signal input means [for each cell] exclusively for receiving the global signal from the global signal generating means; and memory means coupled to receive and store the global signal..." Since the Examiner has not shown the global signal input for each cell, nor a memory means for storing the global signal, we will not

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

sustain the
35 U.S.C. § 102(e) rejection of claim 7, and likewise its dependent claims 8, 9, 10, 21 and 29, which incorporate the unmet limitations noted.

35 U.S.C. § 103 Rejections

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the reasonable teachings or suggestions found in the prior art, or by a reasonable inference to the artisan contained in such teachings or suggestions. In re Sernaker, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." Para-Ordnance Mfg. v. SGS Importers Int'l, Inc., 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995) (citing W. L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)).

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

With regard to claim 6, Appellant argues:

> The final Action acknowledges that the Holsztynski '019 and '474 patents fail to teach or suggest routing a carry or carry/borrow signal **directly to an addressable memory**, but relies on the Morton patent to make up for the deficiencies of Holsztynski. This reliance is unfounded because **Morton does not show any mechanism for writing a carry output to an addressable storage means**. (Emphasis added.) (Brief-page 39.)

At page 13 of the Answer, the Examiner explains how Morton has an addressable memory. However, there is no showing in any of the cited references that "the carry bit from the ALU output is routed to the addressable memory means without passing through any intervening clockable storage means," as recited in claim 6. Again, the Examiner has not shown Appellant's implementation to be shown or suggested by the references of record. Thus, we will not sustain the 35 U.S.C. § 103 rejection of independent claim 6, and likewise claims 20 and 28 which depend therefrom and contain the same unmet limitations.

Claims 4 and 5, which stand rejected with claim 6 as being unpatentable over Holsztynski in view of Morton, are dependent from claim 3, not claim 6. We have decided supra, with respect to the 35 U.S.C. § 102(e) rejection, that Holsztynski does not meet the requirements of claim 3,

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

therefor Holsztynski alone, does not meet the requirements of claims 4 and 5 which depend from claim 3. The inclusion of Morton in the rejection of claims 4 and 5 does not cure this deficiency. Additionally, Morton does not meet the added limitations of claims 4 and 5 as explained with respect to claim 6. Thus, we will not sustain the 35 U.S.C. § 103 rejection of claim 4 and 5.

With respect to independent claim 14 Appellant argues:

> Claim 14 further requires that the means for generating a signal indicative of the equality of first and second multibit operands comprises: a first input for receiving a signal indicative of the equality of a selected bit from the first operand and a selected bit from the second operand; a second input for receiving a signal indicative of the equality of previously compared bits from the first and second operands; means coupled to the first and second inputs for generating a signal indicative of the equality of corresponding portions of the first and second operands, the corresponding portions comprising the selected bit and the previously compared bits from the first and second operands.
>
> It is respectfully asserted that neither of the Batcher or Guttag patents shows this feature. Batcher's equivalence function 60, which was relied on by the final Office Action, merely indicates equivalence between the single-bit values stored in the P and G registers. See Batcher, col. 9, lines 15-20. However, Batcher's equivalence circuit, which includes the gate 138 (having only two inputs) does not provide the ability to factor in the equivalence, or lack thereof, of previously compared bits of multibit operands. To perform a multibit equivalence function, it is necessary, at each clock

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

cycle, to compare not only the two bits currently being clocked through the cell, but also to consider whether all of the

previously considered pairs of bits have also shown equivalence. Consequently, Batcher's equivalence function is incapable of performing the claimed function. (Brief-pages 36 and 37.)

The Examiner responds:

Regarding claim 14 and its dependent claims 15, 24 and 32 and single bit and multibit operation; as stated above; Batcher's lowest level processing elements are single bit devices, however, since they are arranged in an array (rows and columns) Batcher could also be viewed as a column of multibit devices, with the associated multibit operands and masks. Guttag discloses a graphics data processor which has a plurality of bit cells connected together as a multibit apparatus in order to process pixels. Individual bits or fields are masked utilizing transparency masks or plane masks. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide masks appropriate to the data field being processed in order to provide functionality for the intended application, such as image processing, pattern matching etc. The size of the data field (single bit or multibit) being processed would be specific to the intended application. Regarding claims 14-15; Batcher discloses an equivalence function using an (inclusive) OR gate in Col. 9, which has as inputs the P and G registers and outputs a one when the inputs are equal, the output is put on the data bus and can feed the next processing element as the P input to its comparator operation. (Answer-pages 12 and 13.)

Again, the Examiner has not shown Appellant's claimed implementation to be shown or suggested by the cited

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

references. In particular, "a second input for receiving a signal indicative of the equality of **previously compared bits** from the first and

second operands; means coupled to the first and second inputs for generating a signal indicative of the equality of corresponding portions of the first and second operands, the corresponding portions comprising the selected bit and the **previously compared bits** from the first and second operands" as recited in claim 14 (emphasis added) has not been shown. Thus, we will not sustain the 35 U.S.C. § 103 rejection of independent claim 14, and likewise claims 15, 24 and 32 dependent therefrom and containing the same unmet limitation.

Finally, with regard to independent claim 16, The Examiner states:

> Batcher provides coupling i.e. interconnecting the processing elements as described in Col. 4, line 20 et seq.; the P register provides routing functions effectively multi-plexing data sources between the neighboring processing elements and a local data source (RAM). In addition, the adder is described as receiving an input from the shift register, the output of the A register and an input from the P register (Col. 6, line 51 et seq.). In effect, Batcher discloses more structure than applicant, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made that "coupling" may be direct or indirect

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

and any intervening elements chosen (e.g. multiplexing) would be directed toward making the system functional for the intended application. As stated above, a multiplexer is a switch with more than a single input. Batcher provides such switching to pass data from a local data source or from a neighboring data source as described in Col. 9, line 40 et seq. Regarding applicants argument that the multiplexer of claim 16 selects data at one of its inputs to appear at its output in response to a control signal generated within the processing cell, applicants claim 16 processing cell is set forth as having a multiplexer without positively setting forth any data source, local or nonlocal, or any indication or means to generate control signals locally. The elements in claim 16 are as follows: 1) control input means, 2) a plurality of identical processing cells...wherein each processing cell is comprised of a multiplexor. There are no other elements positively set forth. (Answer-pages 11 and 12.)

Appellant argues:

In the present instance, claim 16 does not merely recite a plurality of identical cells, each comprising a multiplexor. To the contrary, claim 16 additionally sets forth that the multiplexor has first and second inputs and an output. Claim 16 further recites a limitation wherein the multiplexor selects data at one of its inputs to appear at its output in response to a control signal generated within the processing cell. Claim 16 still further sets forth a limitation **wherein the first input is coupled to an output of a multiplexor in one of the at least one neighboring cell**, the second input is coupled to a local data source, and the output is coupled to a first input of a multiplexor in one of the at least one neighboring cell. These features cannot be ignored when determining the patentability of claim 16 and its dependent claims 17, 25 and 33 over the prior art. (Emphasis added.) (Reply brief-page 8.)

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

We agree with Appellant. Although the Examiner has shown a multiplexer (or equivalent thereof) in the prior art, and the concept of cell bypassing, the particular arrangement claimed by Appellant is not shown or suggested in the prior art. Claim 16 recites, “a multiplexor having first and second inputs and an output, the multiplexor selecting data at one of its inputs to appear at its output in response to a control signal generated within the processing cell, wherein the first input is coupled to an output of a multiplexor in one of the at least one neighboring cell, the second input is coupled to a local data source, and the output is coupled to a first input of a multiplexor in one of the at least one neighboring cell.” Thus, we will not sustain the 35 U.S.C. § 103 rejection of independent claim 16, and likewise claims 17, 25 and 33 which depend therefrom and contain the same unmet limitations.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84 n.14 (Fed. Cir. 1992), citing In re Gordon, 733 F.2d 900,

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

902, 221 USPQ 1125, 1127 (Fed. Cir. 1984). "Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor." Para-Ordnance Mfg. v. SGS Importers Int'l, 73 F.3d at 1087, 37 USPQ2d at 1239, citing W. L. Gore & Assocs., Inc. v. Garlock, Inc., 721 F.2d at 1551, 1553, 220 USPQ at 311, 312-13.

As pointed out above, the prior art teaches the claimed concepts as known in parallel processor circuits. However, various implementations of these concepts have significant impact on the operational characteristics of the final device. It is here that the prior art fails. Claimed details of Appellant's implementation are not shown or made obvious by the prior art of record. Since there is no evidence in the record that the prior art would have suggested the implementation presented in Appellant's claims, we will not sustain the Examiner's rejections under 35 U.S.C. § 103.

[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

We have not sustained the rejection of claims 3, 7 through 10, 19, 21, 27 and 29 under 35 U.S.C. § 102(e), nor have we sustained the rejection of claims 4, 5, 6, 14 through 17, 20, 24, 25, 28, 32 and 33 under 35 U.S.C. § 103. Accordingly, the Examiner's decision is reversed.

REVERSED

Kenneth W. Hairston)
Administrative Patent Judge) BOARD OF
)
) PATENT
Stuart N. Hecker)
Administrative Patent Judge) APPEALS AND
)
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[1] Application for patent filed August 27, 1993.

[1] Application for patent filed August 27, 1993.

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[1] Application for patent filed August 27, 1993.